D/A and A/D Converters

DIGITAL-TO-ANALOG CONVERTERS

The analog output voltage *VO* of an *N*-bit straight binary D/A converter is related to the digital input by the equation

$$V_O = K(2^{N-1} b_{N-1} + 2^{N-2} b_{N-2} + \ldots + 2^2 b_2 + 2b_1 + b_O)$$

where *K* is a proportionality factor. *bn* = 1 if the *n*th bit of the digital input is 1
= 0 if the *n*th bit of the digital input is 0.

Example 10.1

Find the analog output voltage of a 4-bit D/A converter for all possible inputs. Assume $K = 1$.

Solution

From Eq. (10.1), we obtain the output voltage for each input and these are given in Table 10.1.

Table 10.1

Digital input				Analog output
b_3	b_2	b_1	b_0	V
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3

(*Continued*)

Table 10.1 (*Continued*)

Digital input				Analog output
b_3	b_2	b_1	b_0	V
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

There are two types of commonly used D/A converters. These are:

1. Weighted-resistor D/A converter, and
2. *R*-2*R* ladder D/A converter.

Weighted-Resistor D/A Converter

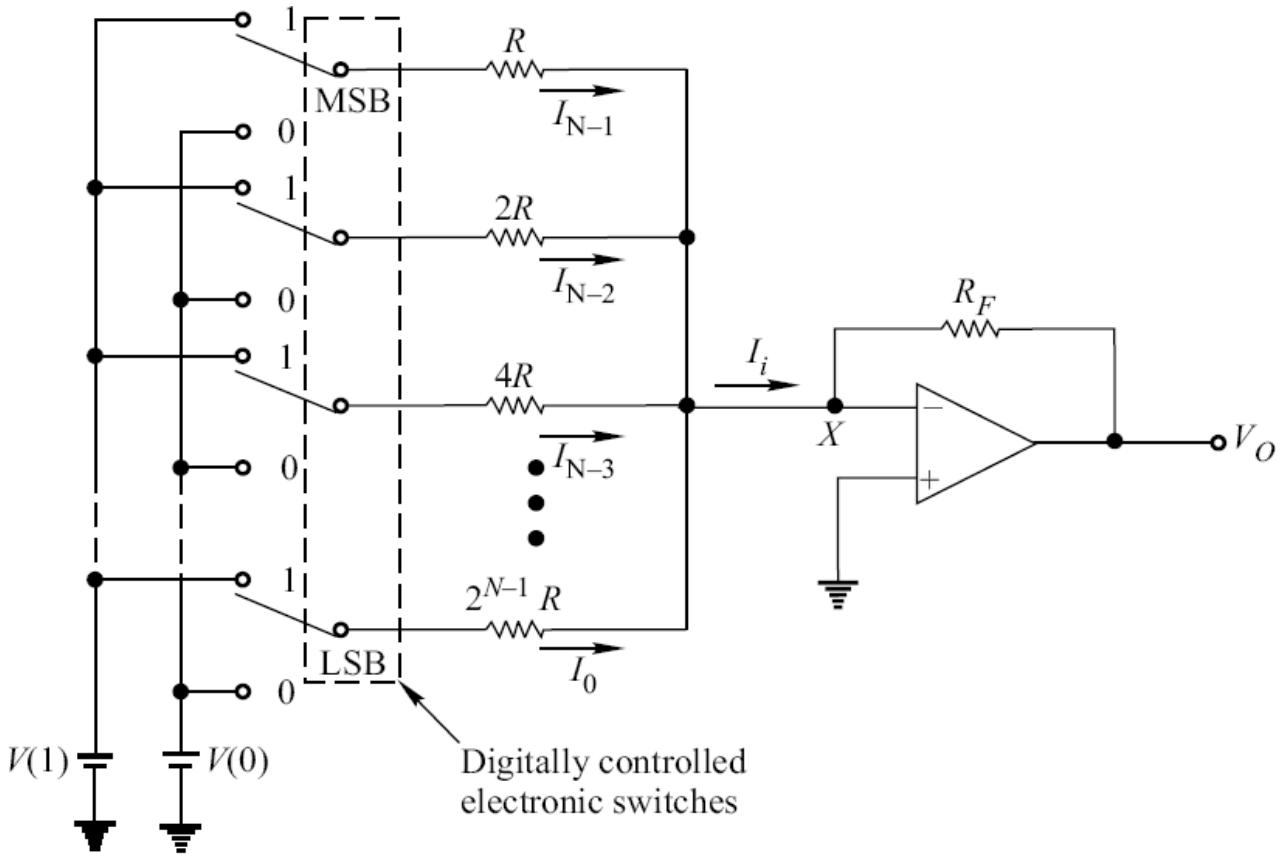


Fig. 10.1 ***Weighted-Resistor D/A Converter***

$$V_O = \frac{R_F}{2^{N-1} R} \left(2^{N-1} V_{N-1} + 2^{N-2} V_{N-2} + \ldots + 2^1 V_1 + 2^0 V_0\right)$$

An offset can also be produced in the output voltage V_O by using the circuit of Fig. 10.2. The offset voltage produced in this circuit is

$$-\frac{R_F}{R_{\text{off}}} \cdot V_{\text{off}}$$

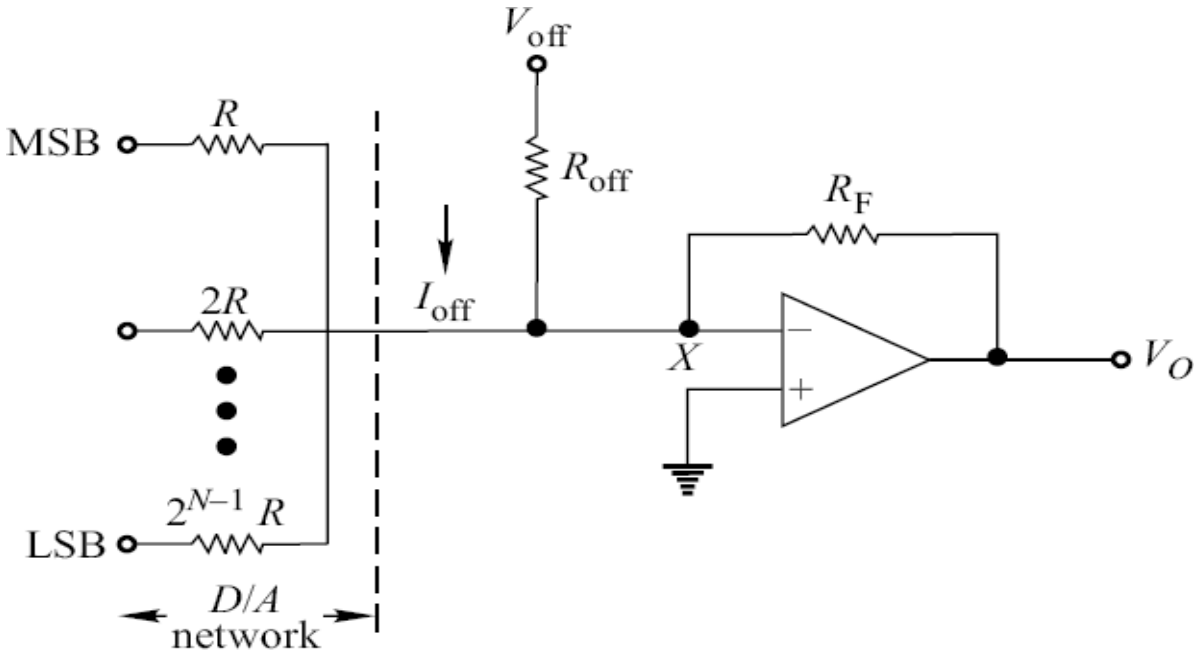


Fig. 10.2 ***Circuit Used to Offset the Output Voltage***

R–2*R* Ladder D/A Converter

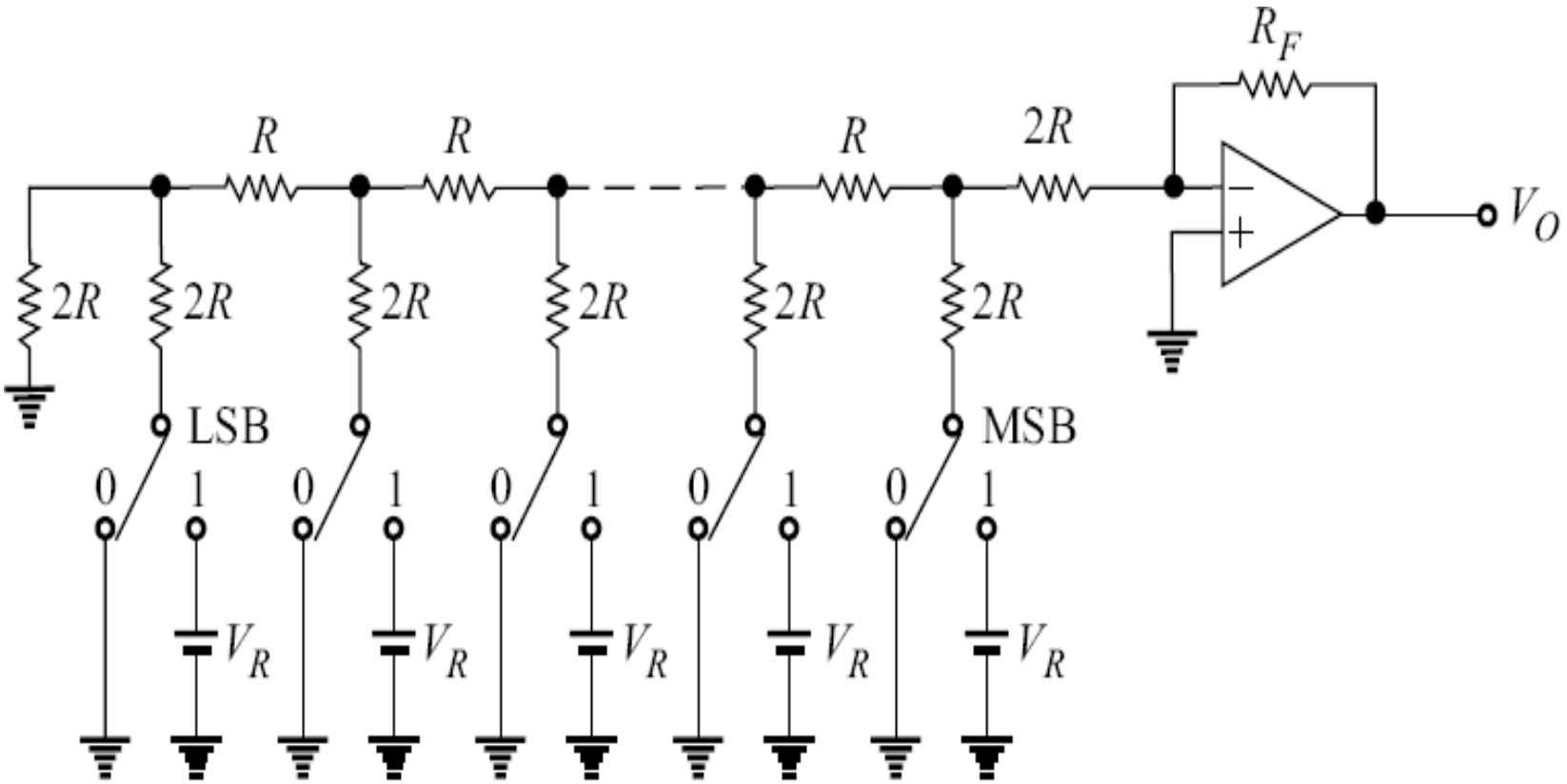


Fig. 10.3 ***R–2R Ladder D/A Converter***

In general, for an *N*-bit D/A converter, the output voltage can be similarly determined and is given by

$$V_O = (2^{N-1}\, b_{N-1} + 2^{N-2}\, b_{N-2} + \ldots + 2^2 b_2 + 2^1\, b_1 + 2^0\, b_0)$$

$$R_F = 3R \text{ and } V_R = -2^N \text{ V}$$

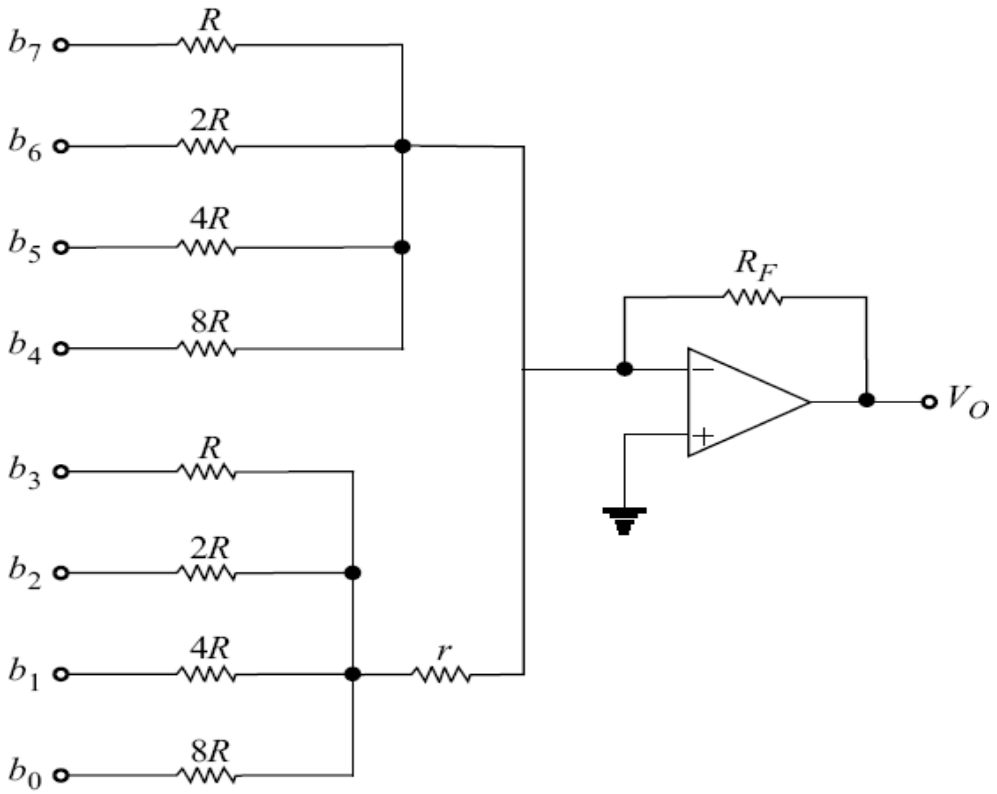


Fig. 10.6 ***Modified Weighted-Resistor D/A Converter***

Specifications for D/A Converters

The characteristics of a D/A converter, which are generally specified by the manufacturers are:
1. Resolution,
2. Linearity,
3. Accuracy,
4. Settling time, and
5. Temperature sensitivity.

These are discussed below:

Resolution

This is the smallest possible change in output voltage as a fraction or percentage of the full-scale output range. An 8-bit D/A converter has an 8-bit resolution.

Linearity

In a D/A converter, equal increments in the numerical significance of the digital input should result in equal increments in the analog output voltage. In an actual circuit, the input–output relationship is not linear. This is due to the error in resistor values and voltage across the switches. The linearity of a converter is a measure of the precision with which the linear input–output relationship is satisfied.

Accuracy

The accuracy of a D/A converter is a measure of the difference between the actual output voltage and the expected output voltage. It is specified as a percentage of full-scale or maximum output voltage. For example, if a D/A converter has 10 V full-scale (maximum) output voltage and an accuracy of ± 0.2%, then the maximum error for any output voltage will be 0.002 × 10 = 20 mV.

Settling Time

The time required for the analog output to settle to within $\pm \frac{1}{2}$ LSB of the final value after a change in the digital input is usually specified by the manufacturers and is referred to as *settling time*.

Temperature Sensitivity

The analog output voltage for any fixed digital input varies with temperature specified as ± ppm/°C.

Parallel-Comparator (or Flash) A/D Converter

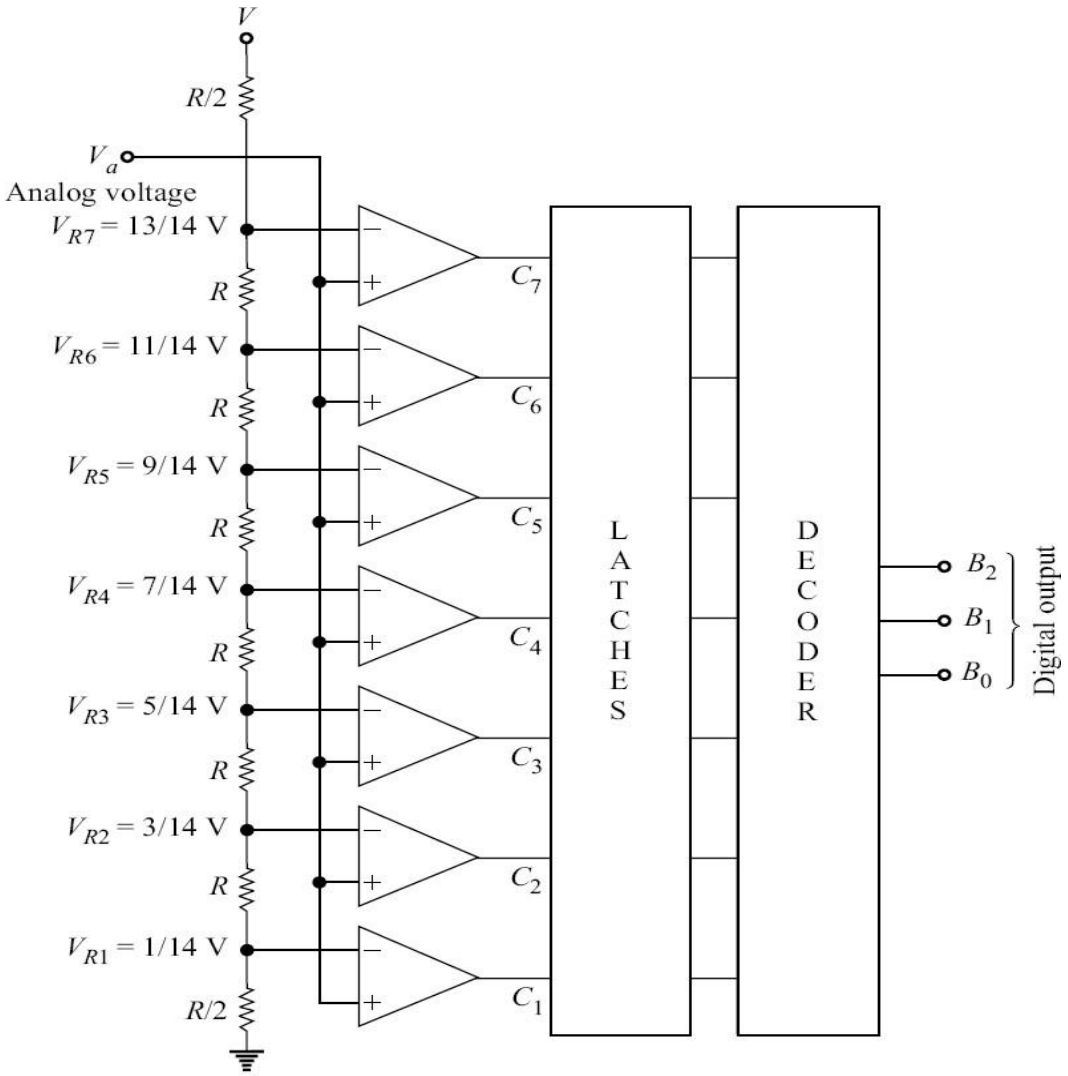


Fig. 10.19 *A 3-bit Parallel-Comparator (Flash) A/D Converter*

Successive-Approximation A/D Converter

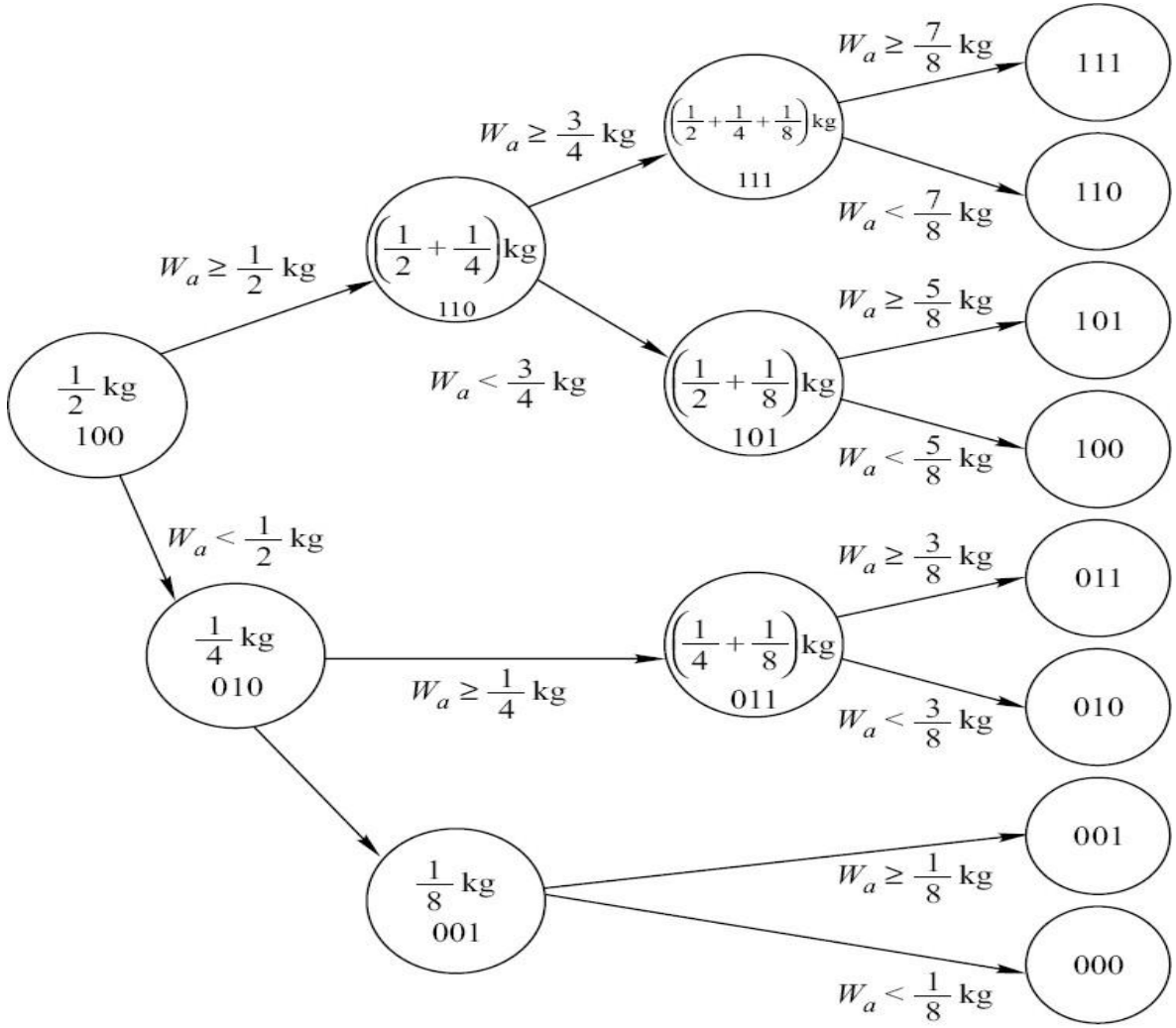


Fig. 10.20 ***Successive-Approximation A/D Conversion Process***

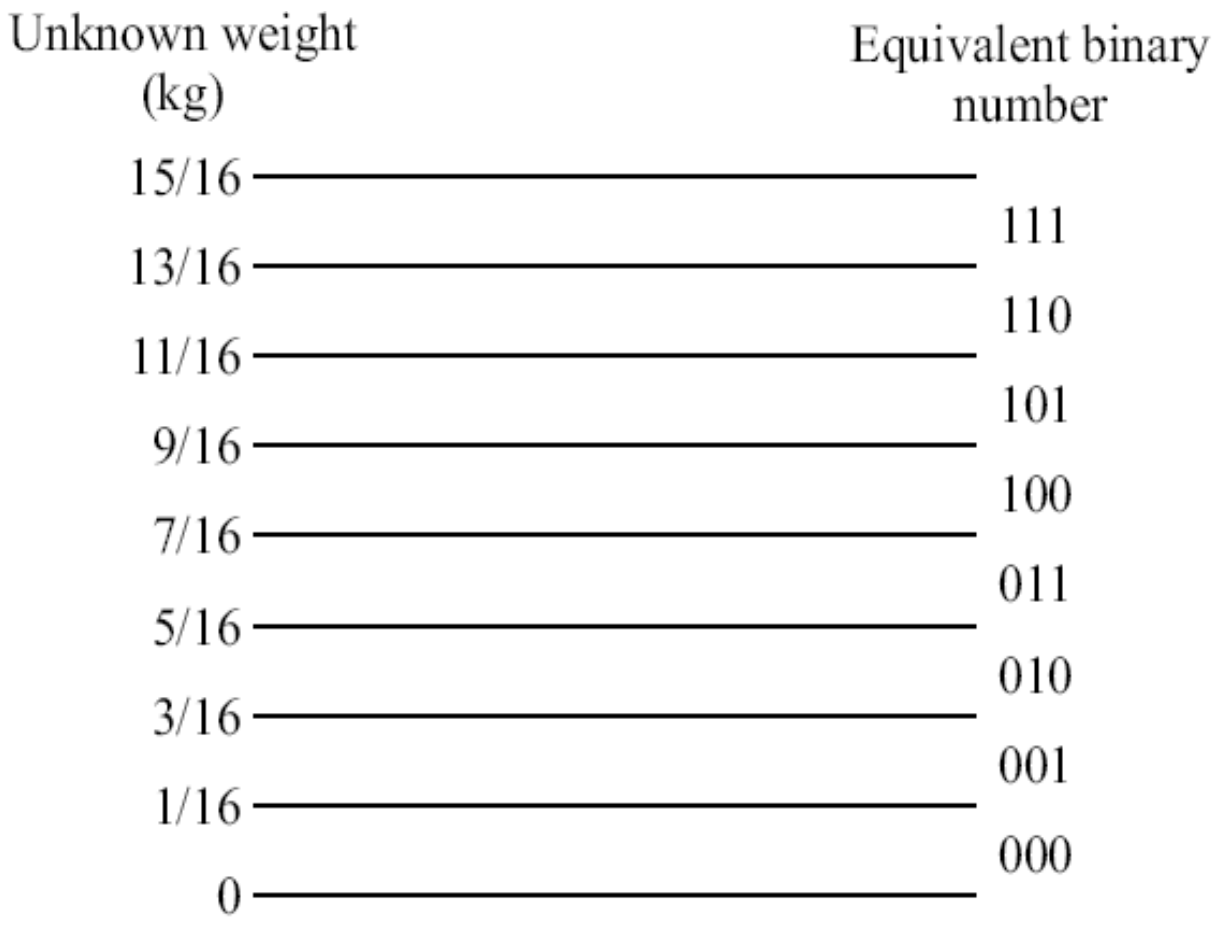


Fig. 10.21 ***Effect of Offsetting the Scale in Successive-Approximation Weighing***

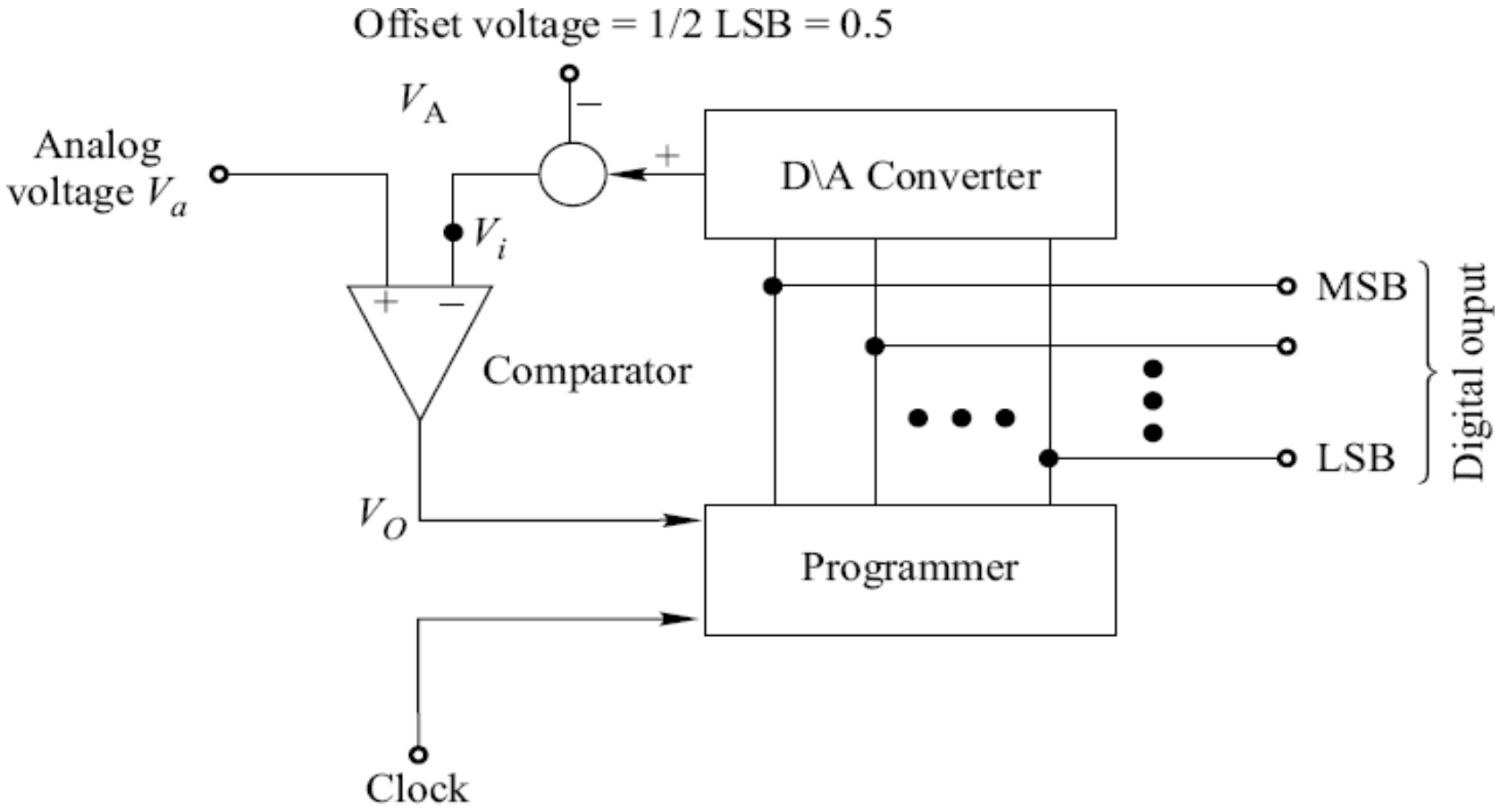


Fig. 10.22 ***Successive-Approximation A/D Converter***

Counting A/D Converter

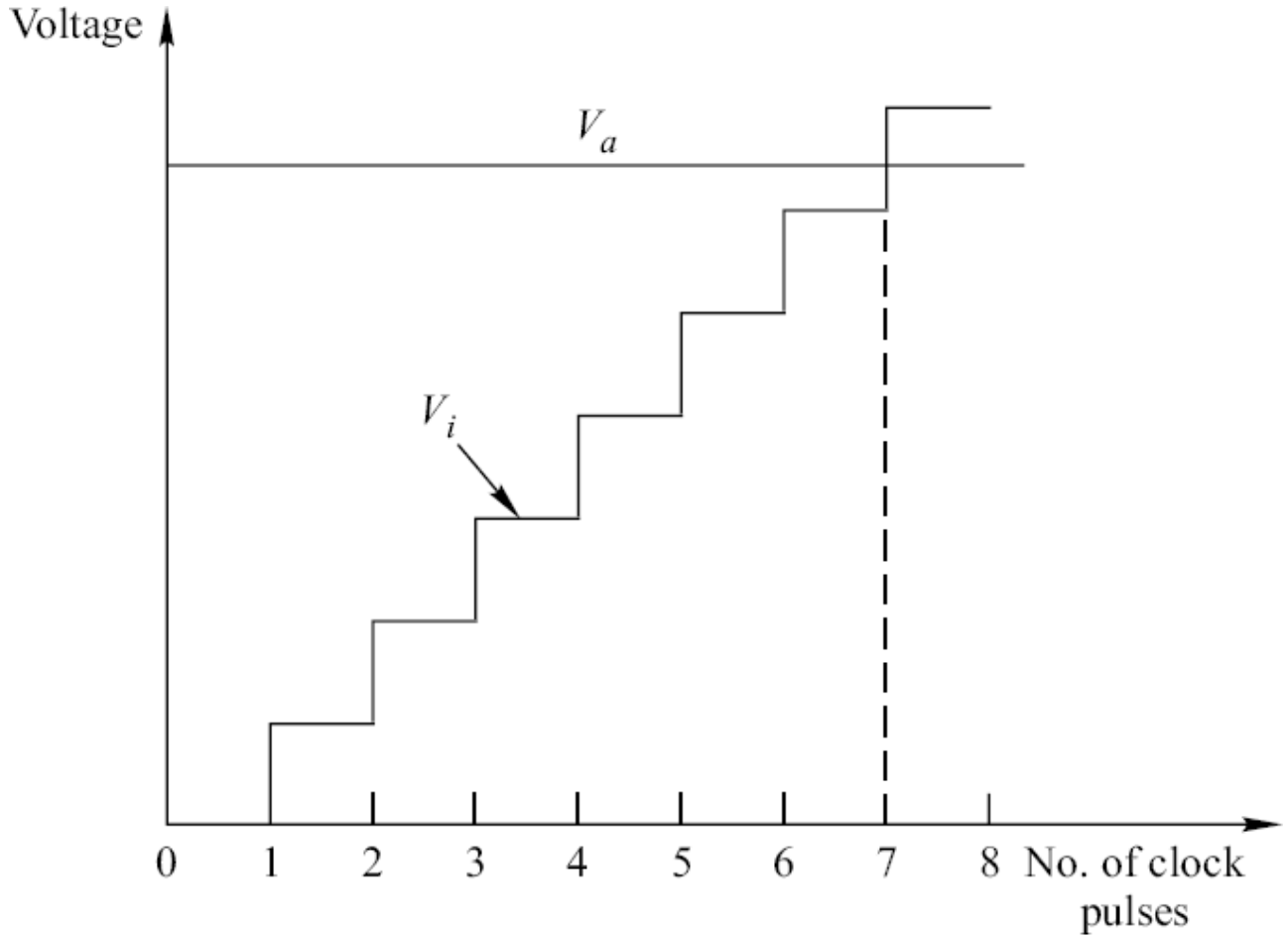


Fig. 10.23 ***Waveform of Counting A/D Converter***

Dual-Slope A/D Converter

The block diagram of a dual-slope A/D converter is shown in Fig.10.24. It has four major blocks:

1. An integrator,
2. A comparator,
3. A binary counter, and
4. A switch driver.

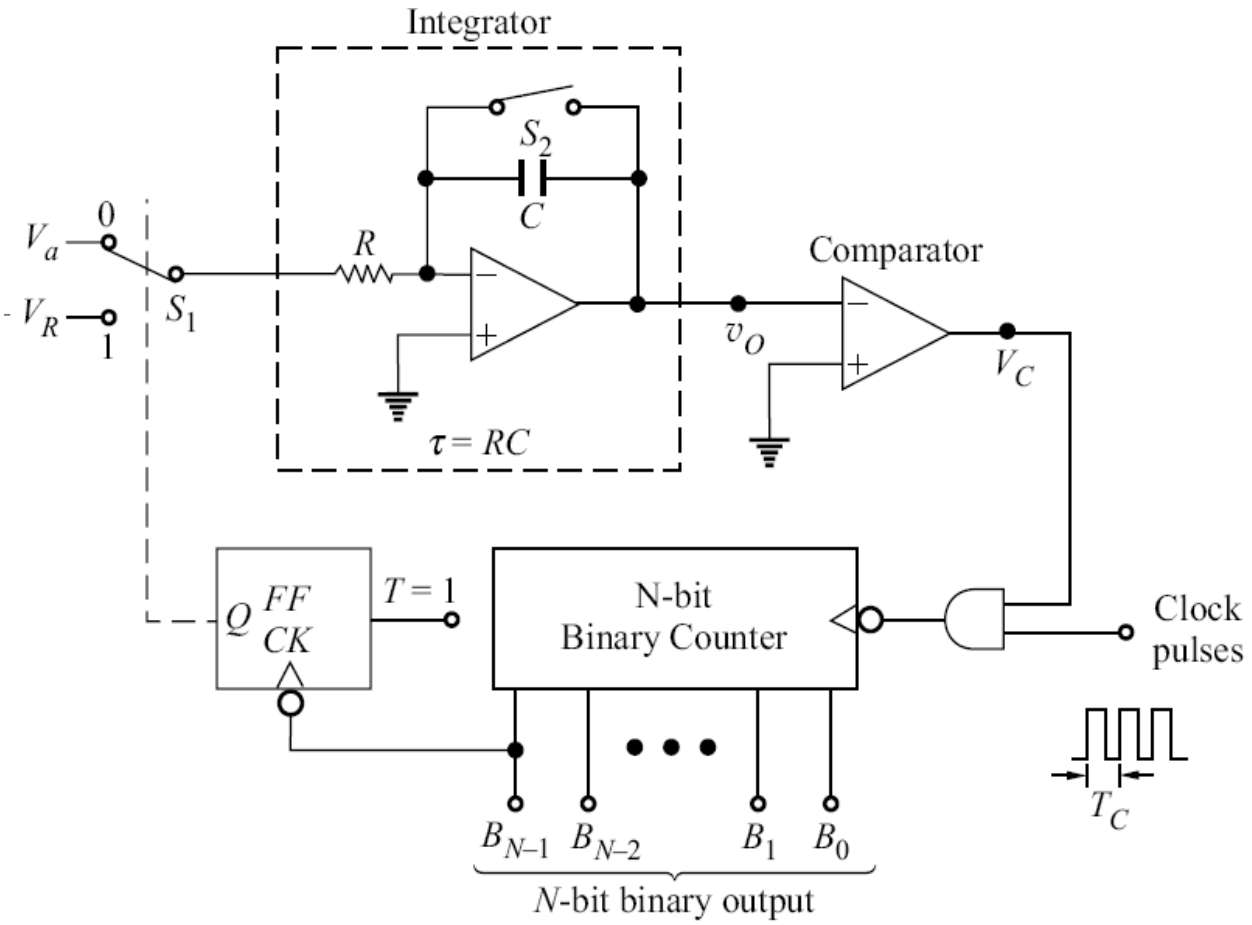


Fig. 10.24 ***Dual-Slope A/D Converter***

$$n = \frac{V_a}{V_R} \cdot 2^N$$

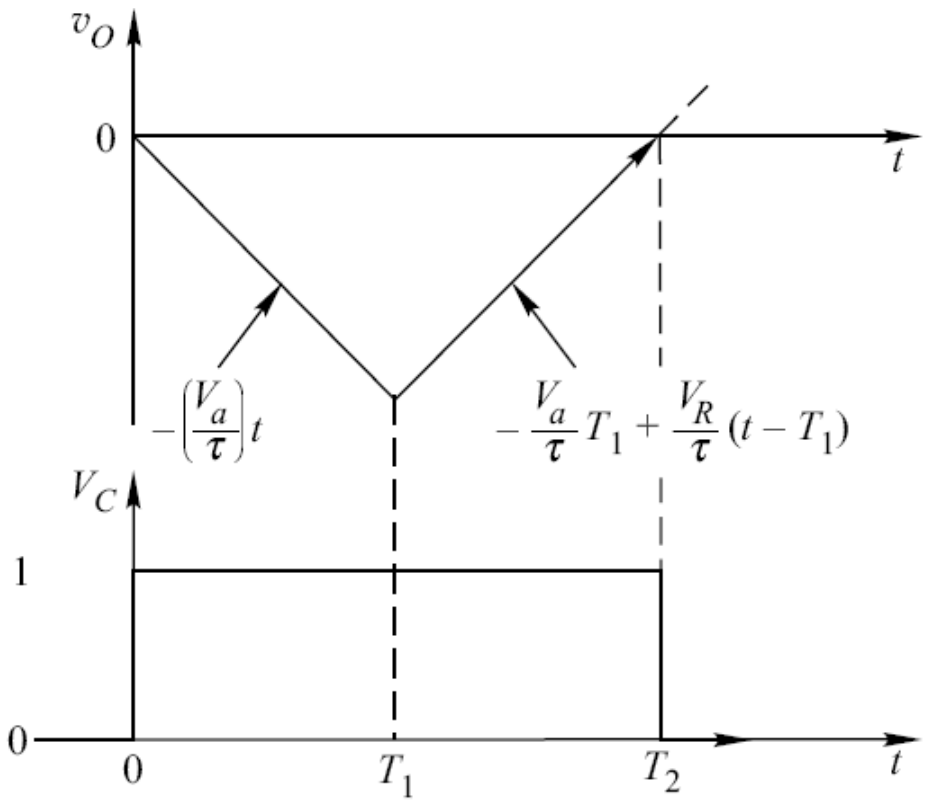


Fig. 10.25 ***Waveforms of Dual-Slope A/D Converter***

This type of A/D converter is often used in digital voltmeters because of its good conversion accuracy and low cost. The disadvantage of the dual-slope A/D converter is its slow speed.

4.1.2 Unipolar Logic Families

MOS devices are unipolar devices and only MOSFETs are employed in MOS logic circuits. The MOS logic families are:

1. PMOS,
2. NMOS, and
3. CMOS (5-V and low-voltage CMOS)

While in PMOS only *p*-channel MOSFETs are used and in NMOS only *n*-channel MOSFETs are used, in complementary MOS (CMOS), both *p*- and *n*-channel MOSFETs are employed and are fabricated on the same silicon chip.

4.1.3 BiCMOS Logic Family

BiCMOS logic circuits use CMOS devices for input and logic operations and bipolar devices for output.

Wired-Logic

If the outputs of the gates are connected together as shown in Fig. 4.6, the output *Y* is given by

$$\begin{aligned} Y &= Y_1 \cdot Y_2 \\ &= \overline{A + B} \cdot \overline{C + D} \\ &= \overline{A + B + C + D} \end{aligned}$$

This shows that fan-in can be increased by this connection which is referred to as *wired-* AND or *implied-*AND.

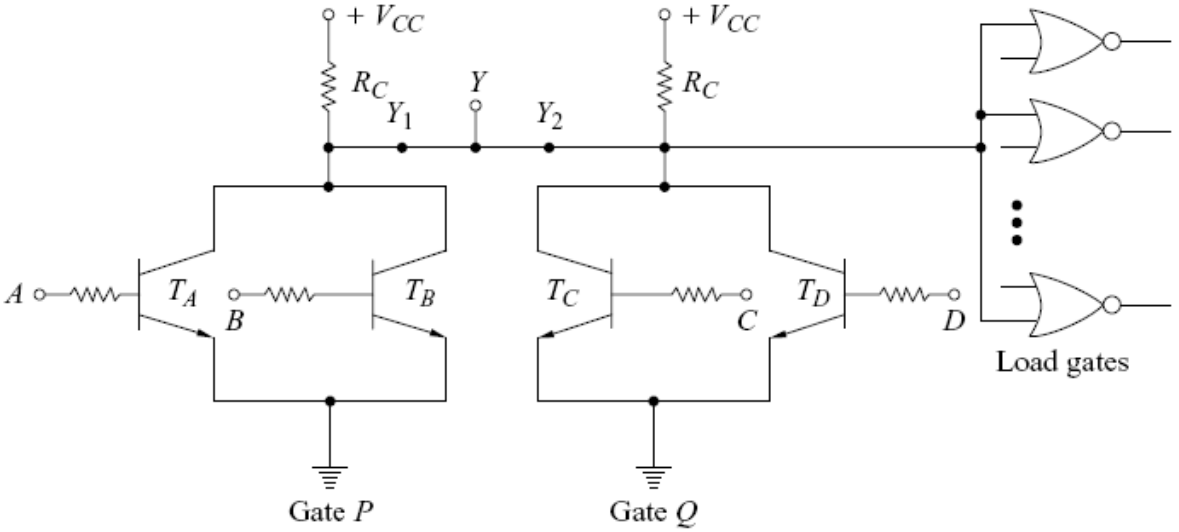


Fig. 4.6 ***Wired-AND Connection of RTL Gates Driving Similar Gates***

TRANSISTOR – TRANSISTOR LOGIC (TTL)

The transistor–transistor logic (TTL) is the most successful bipolar logic which was evolved in the 1960s. TTL families use transistors, both to perform logic functions and to provide high output drive capability.

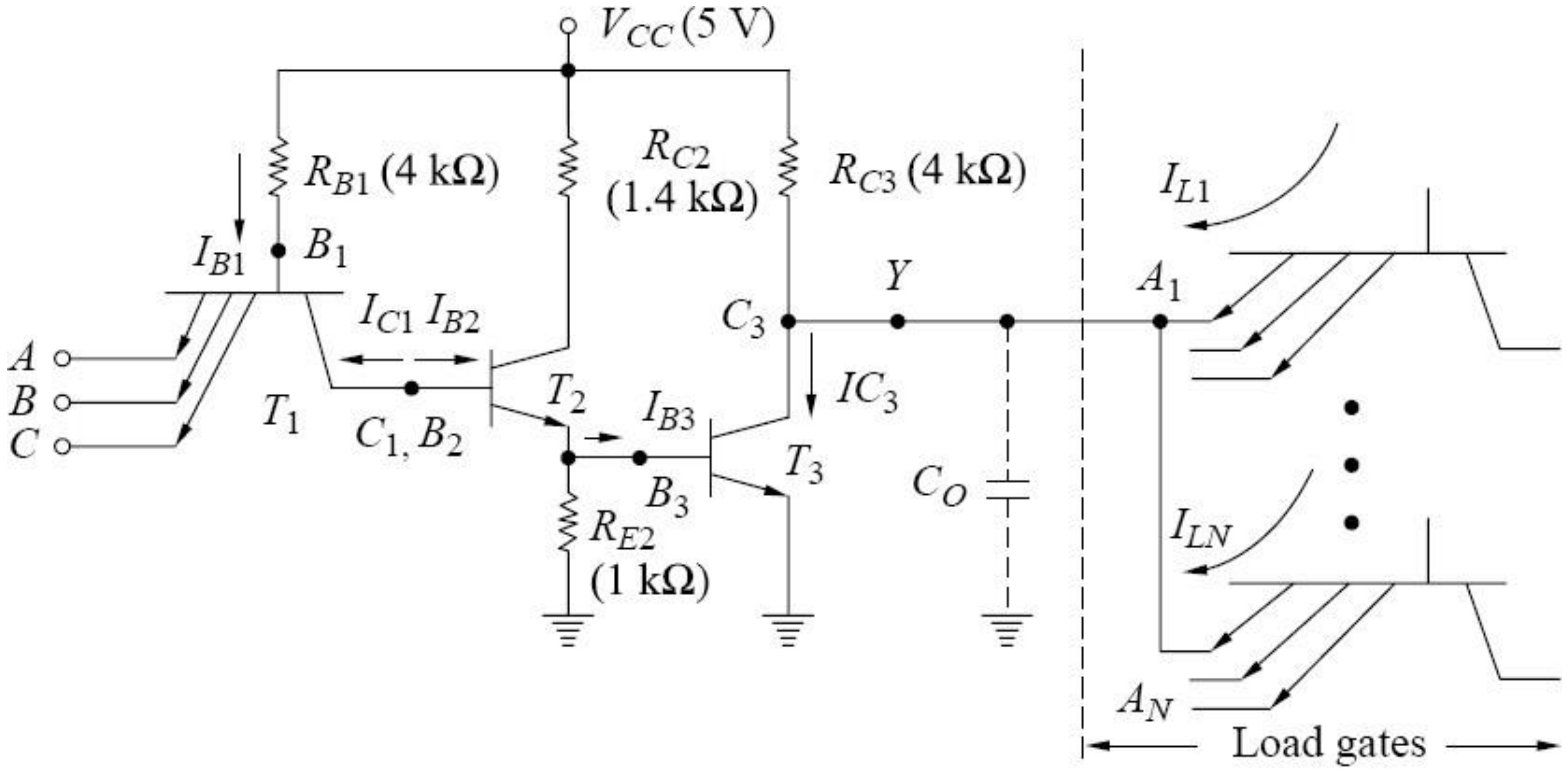


Fig. 4.16 *A 3-Input TTL* NAND *Gate Driving N Similar Gates*

Operation of TTL NAND GATE

Let us assume that the load gates are not present and the voltages for logic 0 and 1 are $V_{CE,sat} \approx 0.2$ V and $V_{CC} = 5$ V respectively.

The following voltages are assumed for *p-n* junction (diode operation) and transistors.

p-n junction: Voltage across a conducting diode = 0.7 V
Cut-in voltage $V_r = 0.6$ V

Transistor: Cut-in voltage $V_r = 0.5$ V
$V_{BE,sat} = 0.8$ V
$V_{CE,sat} = 0.2$ V

Condition I At least one input is LOW. The emitter–base junction of T_1 corresponding to the input in the LOW state is forward-biased making voltage at B_1, $V_{B1} = 0.2 + 0.7 = 0.9$ V. For base–collector junction of T_1 to be forward-biased, and for T_2 and T_3 to be conducting, V_{B1} is required to be at least $0.6 + 0.5 + 0.5 = 1.6$ V. Hence, T_2 and T_3 are OFF.

Since T_3 is OFF, therefore $Y = V(1) = V_{CC}$.

Figure 4.17*a* illustrates the circuit corresponding to this condition.

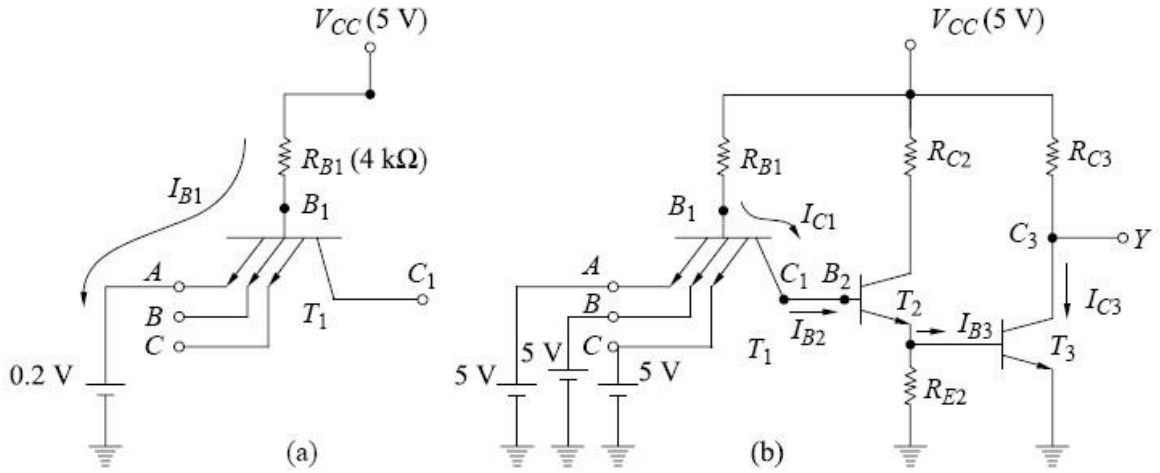


Fig. 4.17 ***Circuits Illustrating the Operation of TTL NAND Gate. (a) Atleast One of the Inputs is LOW (b) All the Inputs are HIGH***

Condition II All inputs are HIGH. The emitter–base junctions of T_1 are reverse-biased. If we assume that T_2 and T_3 are ON, then $V_{B2} = V_{C1} = 0.8 + 0.8 = 1.6$ V. Since B_1 is connected to V_{CC} (5 V) through R_{B1}, the collector–base junction of T_1 is forward-biased. The transistor T_1 is operating in the active inverse mode, making I_{C1} flow in the reverse direction. This current flows into the base of T_2 driving T_2 and T_3 into saturation. Therefore, $Y = V(0) \approx 0.2$ V.

Figure 4.17(b) Illustrates the circuit corresponding to this condition.

The above operation shows that the gate of Fig. 4.16 operates as a NAND gate. From conditions I and II, it appears that T_1 is acting as back-to-back diodes. The importance of T_1 will become clear from condition III.

Condition III Let the circuit be operating under condition II when one of the inputs suddenly goes to $V(0)$. The corresponding emitter–base junction of T_1 starts conducting and V_{B1} drops to 0.9 V. T_2 and T_3 will be turned off when the stored base charge is removed. Since $V_{C1} = V_{B2} = 1.6$ V, therefore the collector–base junction of T_1 is back-biased, making T_1 operate in the normal active region. This large collector current of T_1 is in a direction which helps in the removal of stored base charge in T_2 and T_3 and improves the speed of circuit. The direction of the collector current is same as the current I_{C1} shown in Fig.4.16. The output voltage is pulled-up by the time constant $T = R_{C3} \cdot C_o$. Resistance R_{C3} is known as *pull-up resistor*.

EMITTER-COUPLED LOGIC (ECL)

Emitter-coupled logic (ECL) is the fastest of all logic families and therefore is used in applications where very high speed is essential.

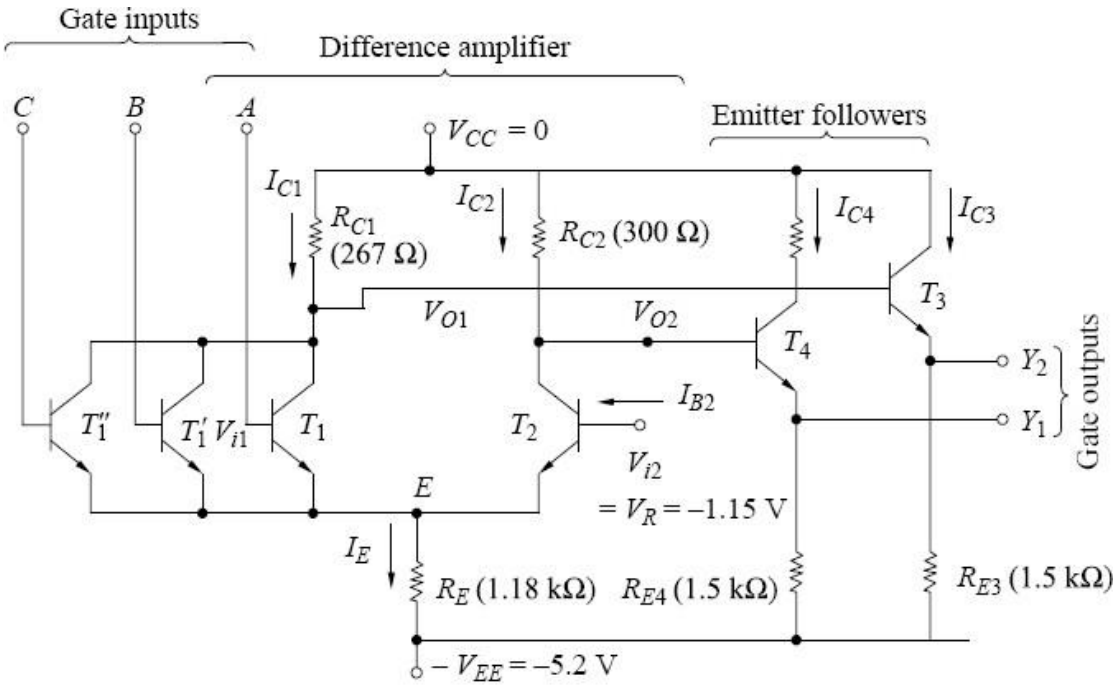
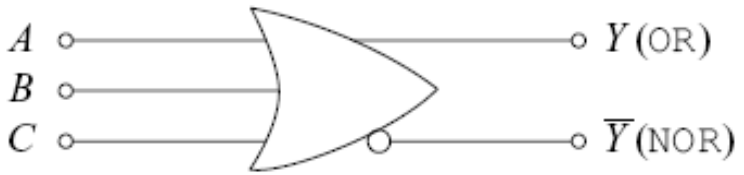


Fig. 4.21 ***A 3-Input ECL*** OR/NOR ***Gate***



The Symbol for a 3-Input OR/NOR ***Gate***

MOS LOGIC

MOS Inverter

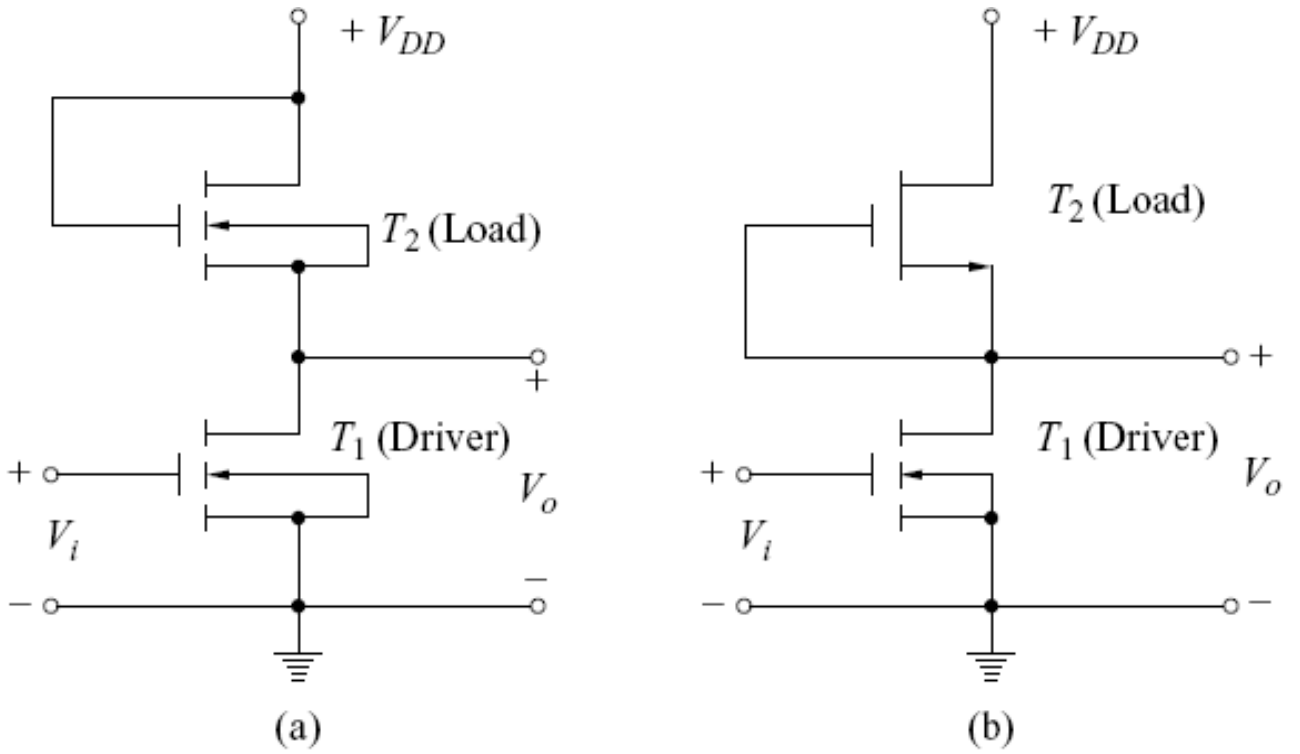


Fig. 4.27 ***A MOS Inverter with (a) Enhancement Load (b) Depletion Load***

The logic levels for the MOS circuits are

$$V(0) \approx 0$$

$$V(1) \approx V_{DD}$$

MOSFET NAND **and** NOR **Gates**

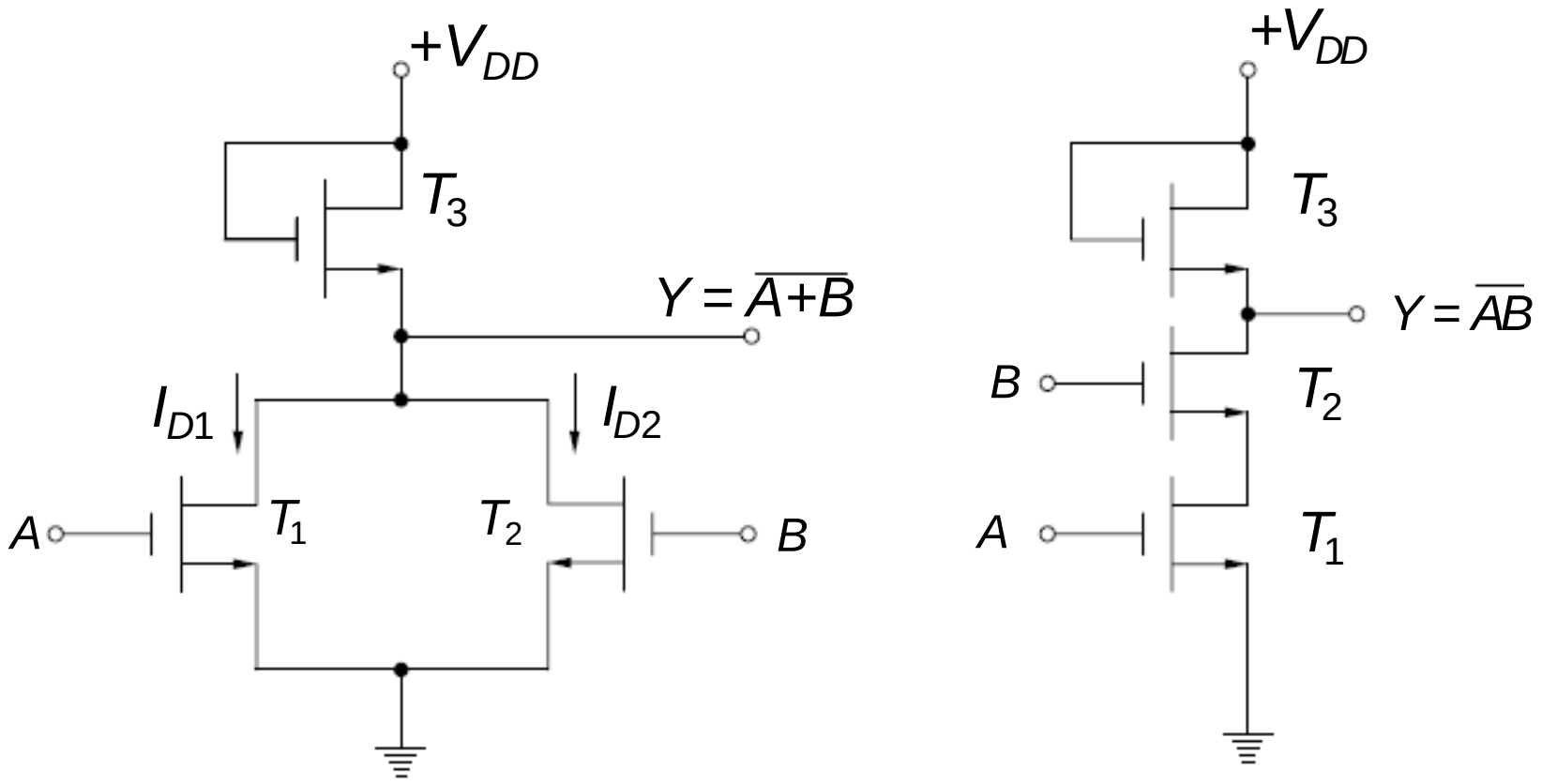


Fig. 4.28 ***2-Input NMOS Gates (a)*** NOR ***(b)*** NAND

CMOS LOGIC

CMOS Inverter

The basic CMOS logic circuit is an inverter shown in Fig. 3.35.

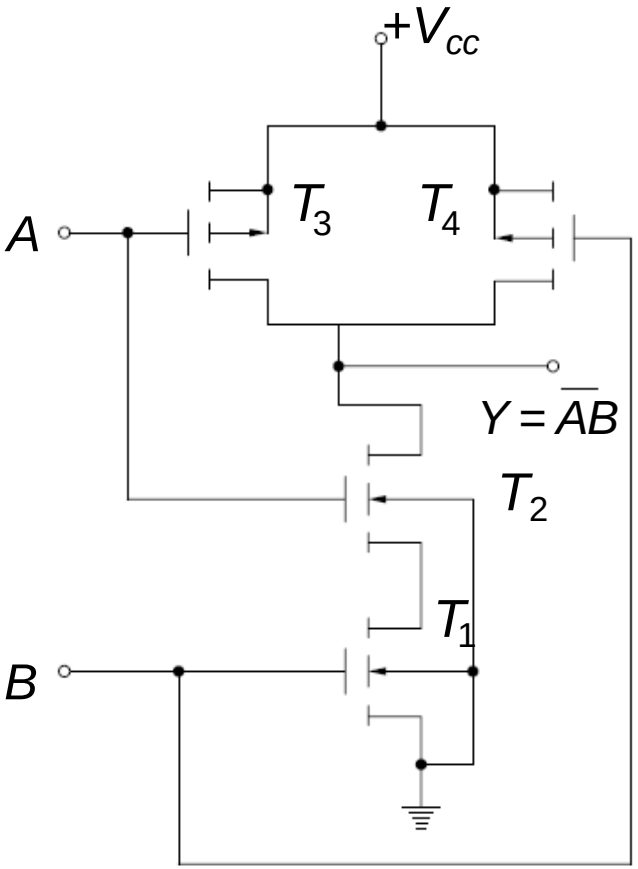


Fig. 4.29 *A 2-Input CMOS* NAND *Gate*

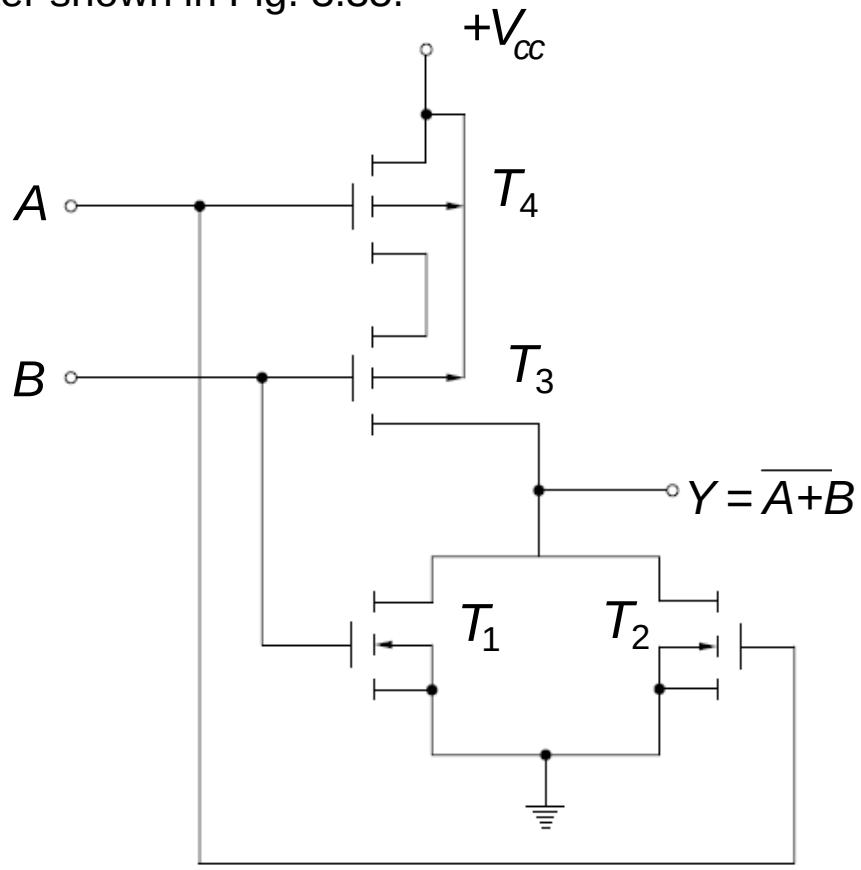


Fig. 4.30 *A 2-Input CMOS* NOR *Gate*

Operation of CMOS NAND *Gate*

Inputs		State of MOS devices				Output
A	*B*	T_1	T_2	T_3	T_4	*Y*
0	0	OFF	OFF	ON	ON	V_{CC}
0	V_{CC}	ON	OFF	ON	OFF	V_{CC}
V_{CC}	0	OFF	ON	OFF	ON	V_{CC}
V_{CC}	V_{CC}	ON	ON	OFF	OFF	0

CMOS Non-Inverting Buffer

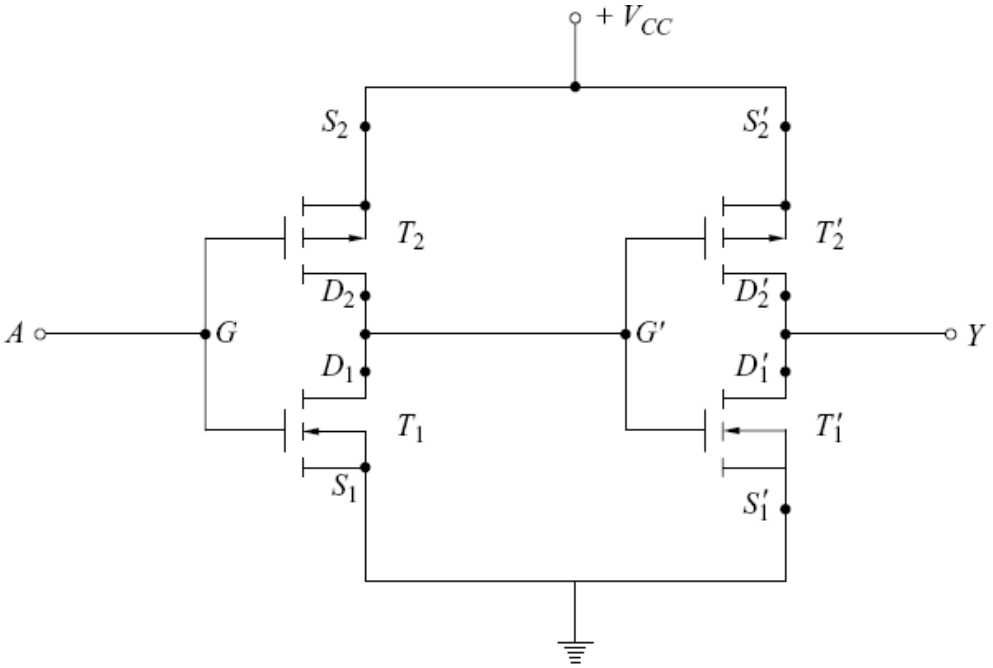


Fig. 4.31 ***Internal Structure of a CMOS Non-Inverting Buffer***

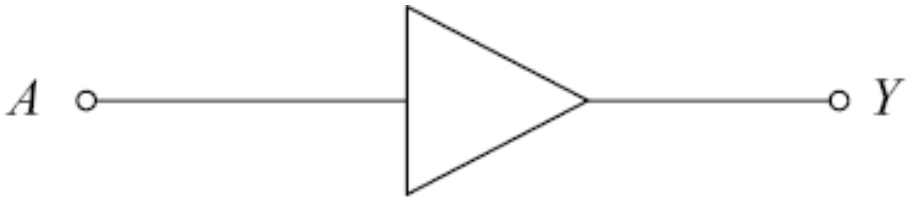


Fig. 4.32 ***Logic Symbol of a Non-Inverting Buffer***

Table 4.9 ***Operation of CMOS Non-inverting Buffer***

Input	**State of MOS devices**				**Output**
A	T_1	T_2	T'_1	T'_1	Y
0	OFF	ON	ON	OFF	0
V_{CC}	ON	OFF	OFF	ON	V_{CC}

CMOS AND **and** OR **Gates**

Similar to CMOS non-inverting buffer, CMOS AND and OR gates are obtained by connecting an inverter to the output of the NAND gate of Fig. 4.29 and the NOR gate of Fig. 4.30 respectively.

Wired-Logic

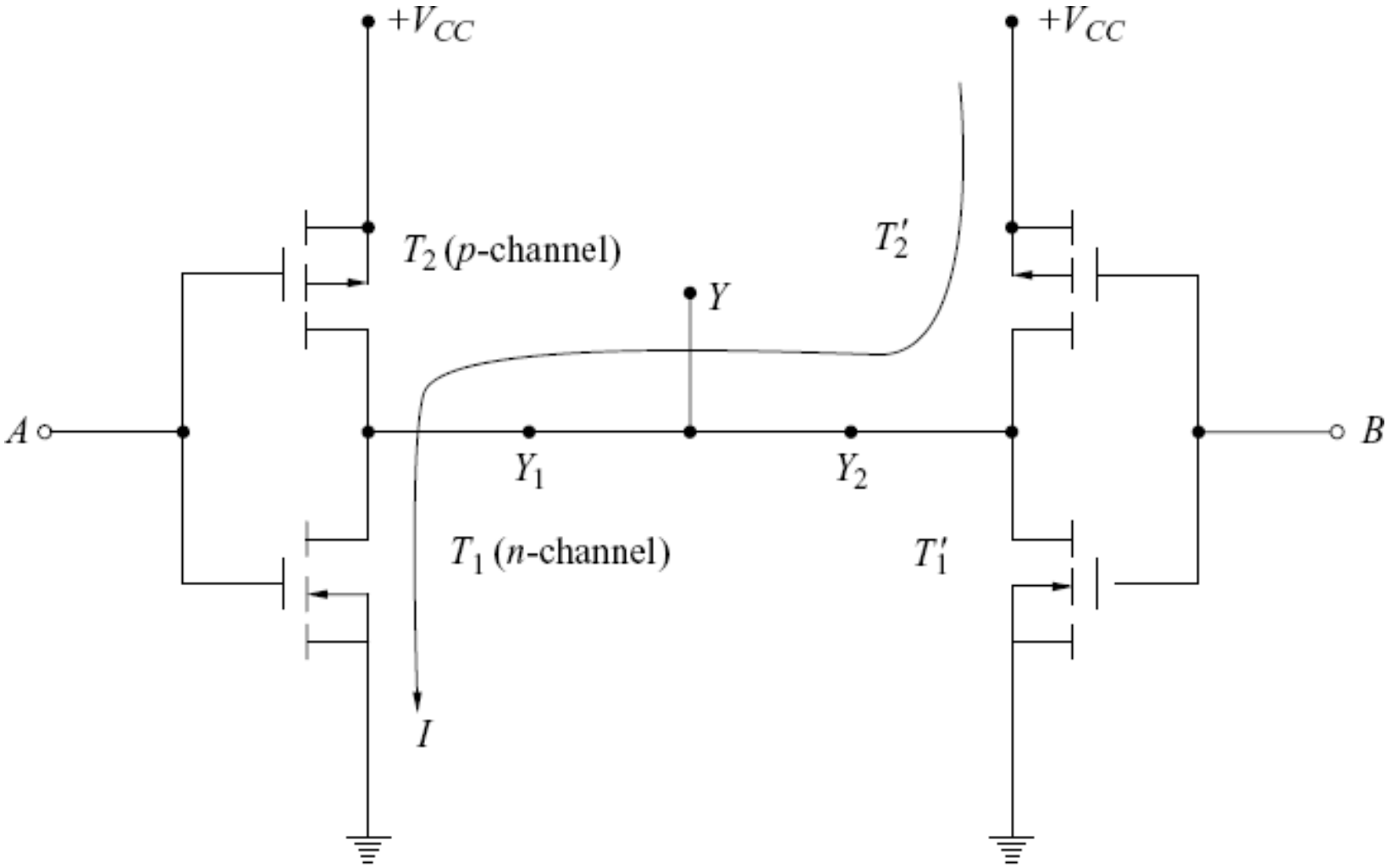


Fig. 4.36 ***CMOS Inverters with Outputs Connected***